ComSysDes

COMMUNICATION SYSTEMS DESIGN LLC

http://www.comsysdes.com
Voice & fax 510-792-1760

66 Santos Court
Fremont, CA 94536 - USA

High Speed Data Transfer in Backplanes & Cables

Available Technology Choices

Terry Fernandes

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ComSysDes
http://www.comsysdes.com
Voice & fax 510-792-1760

COMMUNICATION SYSTEMS DESIGN LLC
66 Santos Court
Fremont, CA 94536 - USA

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Scope of this Report

This report details the results of studying the available technology options for designing a high-speed data transfer environment. Moving high speed digital data, whether through a PCB (Printed Circuit Board), or across cable, requires a solution that:

- is immune from noise
- generates very little noise to satisfy EMI requirements
- consumes as little power as possible
- is easy to implement
- is low cost

This study focuses on the choices of the driving and receiving logic to satisfy the above requirements.

Reader feedback is appreciated and encouraged. Please address your comments or requests to Mktg@ComSysDes.com,

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Technologies Available for High-Speed Data Transfer Designs

In any high-speed data transfer environment, the two primary issues that must be considered are speed and distance. There are several standards that address these issues, such as EIA-232/422/485, LVDS, and USB. Attention will only be given to high-speed point-to-point parallel applications.

There are currently two configurations in which data is transferred in any given environment, *single-ended* and *differential*.

Single-Ended Data Transfers

Single-ended transfers take place on a single line, referenced to ground. The primary advantages using the Single-Ended technology are:

- a single line (trace) is required per signal
- implementation costs are lower due to :

1. lower connector pin count, which can result in using fewer connectors.
2. signal trace count is low.
3. PCB routing is less complicated.

Since Single-ended data transfers are referenced to ground, one of the major disadvantages is poor noise immunity. Other potential pitfalls include higher levels of cross talk, and higher radiated EMI noise levels (EMI - Electro-magnetic interference).

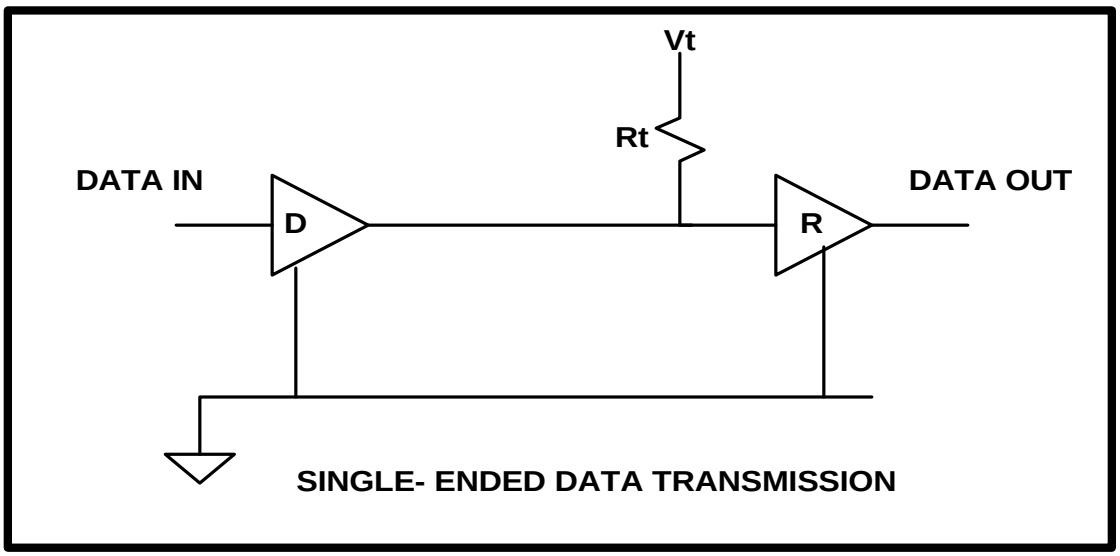

Figure 1: Single Ended Transmission

Logic Families for Single-Ended High Speed Data Transfers

One of the logic families that is utilized in Single-Ended applications, and capable of operating at data rates in excess of 50 MHz is *Gunning Transceiver Logic (GTL)*. GTL is an open-drain/open-collector technology, similar to existing TTL/LVTTL, but operates at a reduced voltage-swing (typically less than 1V). Moreover, because its structure is open-drain/open-collector, GTL requires that the signal trace be actively terminated to the terminating voltage for proper signaling.

A more robust variant of GTL, *GTLP (Gunning Transceiver Logic Plus)*, can handle data rates beyond 80 MHz. The one main characteristic that distinguishes GTLP from GTL is that GTLP incorporates Output Edge-Control circuitry that enables slowing the signal edge-rate. The voltage swings of GTLP are also small compared to GTL, typically between 1.5V and 0.5V with +/-50mV around the 1V Reference Voltage. Finally, the output termination voltage of GTLP is 1.5V, compared to 1.2V of GTL.

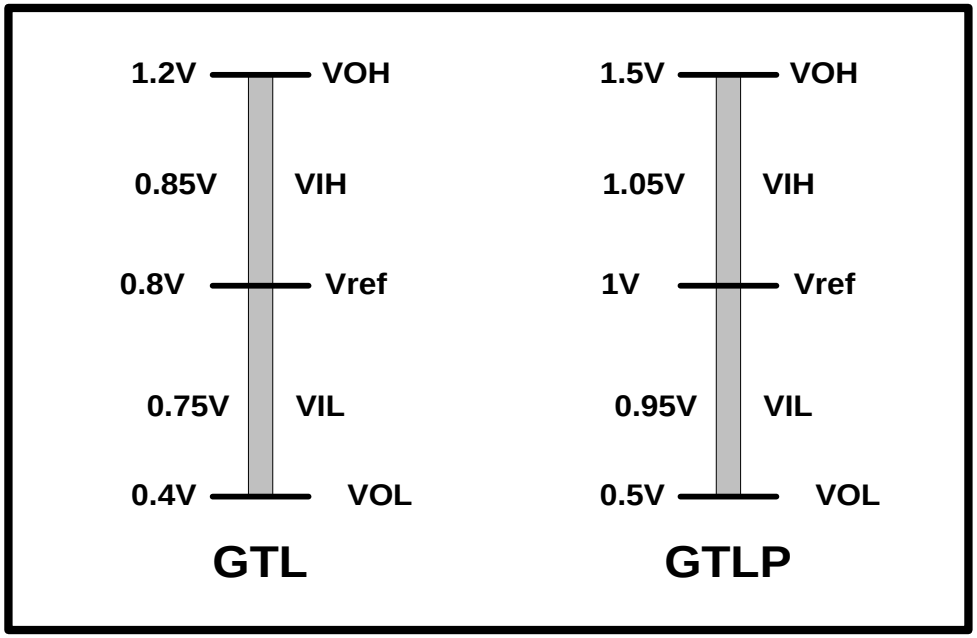

Figure 2: GTL & GTLP levels

The termination requirements for GTLP are such that termination resistors be present on both ends of the signal trace, and pulled up to a termination reference voltage of 1.5V. Typical values for the termination resistor vary between 20 to 40 ohms, and are dependent on the number of loads (ex. backplane slots), as well as, the characteristic impedance of the medium (PCB). The rule here is that, the higher the number of loads (slots), the lower the terminating resistor value.

Since GTLP devices can have slower edge rates, they are best suited for parallel backplane applications.

Unused TTL inputs (A-port) on the GTL/GTLP devices require either a 1K pull-up to Vcc, or a 220-ohm pull-down to GND. Unused inputs on the GTLP side (B-port) should be tied to ground through a 220-ohm resistor.

Vendors such as *Texas Instruments, Fairchild and Pericom, specialize in both GTL, as well as, GTLP logic.*

Differential Data Transfers

Differential Data transfers take place on a pair of signal traces, on which one trace carries the true signal, while the other trace carries the same signal, only inverted. Noise visible on both lines of the pair, appear as common-mode noise, i.e. both traces have equal noise levels. Taking advantage of the common-mode rejection characteristics of any differential amplifier (receiver), it can be shown that the noise rejection performance of a differential transfer system is much higher compared to a single-ended system.

Another advantage in the differential scheme, is the lower amount of radiated noise (EMI) levels. This is due to the opposing electromagnetic fields in each pair of signals, canceling each other out.

Since it takes a pair of wires to transfer any serial data, the use of specialized connectors specifically designed for high-speed differential data transfers is necessary. This requirement adds to the cost of Differential data transmission making it higher compared to Single Ended transmission. However, using the right logic family, as well as, using proper termination techniques, data rates in excess of hundreds of megabits per second can be achieved using a differential scheme.

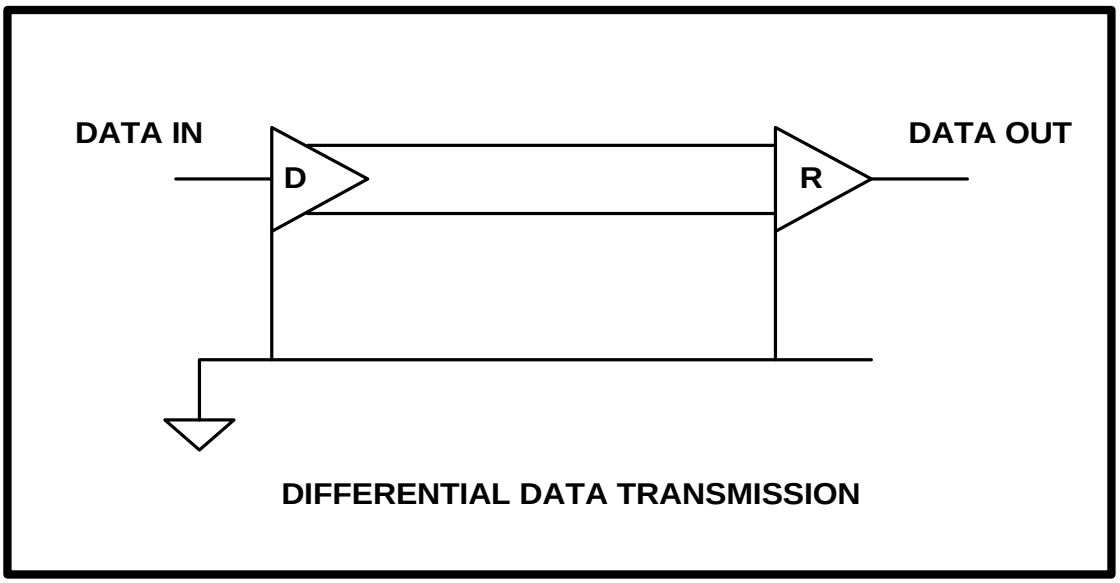

Figure 3: Differential data transmission

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Logic Families for Differential High-Speed Data Transfers

Two logic families that were designed specifically for Differential high-speed serial data transfers are *LVDS (Low Voltage Differential Signaling)* and *PECL (Positive Emitter Coupled Logic).*

LVDS signal characteristic is the low amplitude, with voltage swing of approximately 350mV (typical), generated on a 100-ohm termination resistor. Since LVDS drivers are current-mode types, they consume very little power, and therefore, create less noise (EMI) than their counterparts. The recommended maximum data rate in point to point applications using LVDS is in the order of 655Mbps, but is also dependent on the characteristics of the PCB.

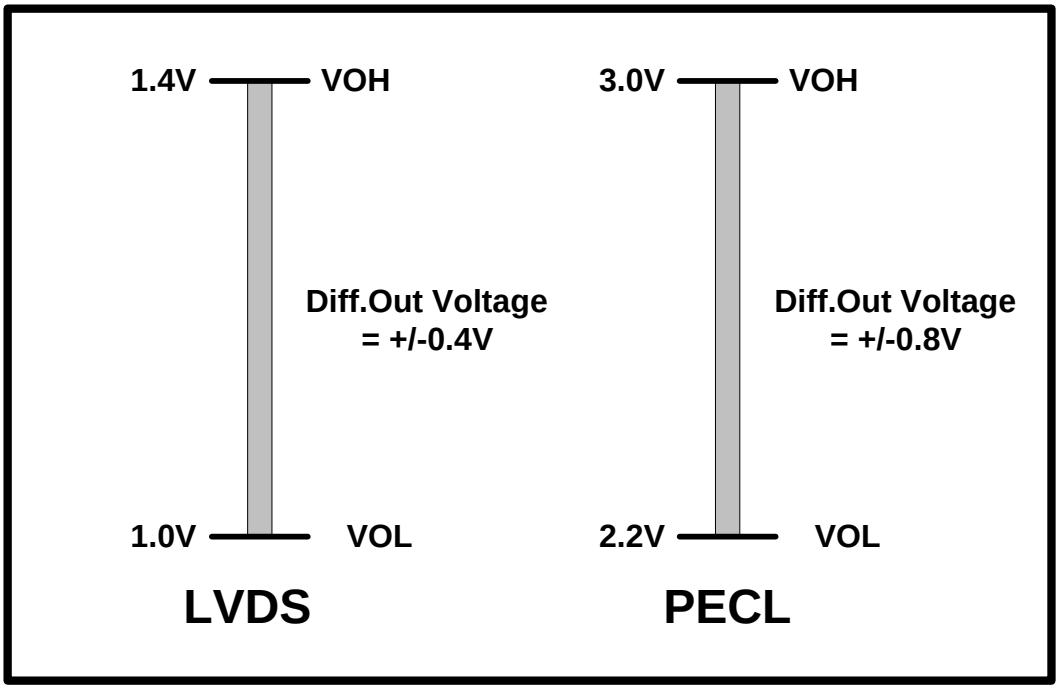

Figure 4: LVDS & PECL levels

LVDS Receivers have built in failsafe circuitry that forces the output to a known logic state, (usually to a logic High), in the event of an open, or short on the receiver inputs. In a noisy environment (more noise than the internal failsafe circuitry can overcome), the receiver may oscillate. By adding a pull-up resistor on the positive input of the receiver, and an equivalent pull-down resistor on the negative input (typical resistor value is 300K), additional failsafe current is

provided to the receiver input. However, this is a compromise between adding failsafe and somewhat degrading signal quality

For multi-point applications, LVDM (Low Voltage Differential Signaling-multi-point) logic is used. LVDM, also referred to as Bus LVDS, has twice the driver output current of LVDS, and requires 100-ohm termination resistors on both ends of the transmission line.

Another logic family designed to operate in the high-speed Differential-signaling environment is PECL.

PECL differs from LVDS in that its voltage swings are typically in the order of 800mV. PECL's power consumption is higher, its noise immunity is lower, and it requires a more complex termination scheme than just the single 100-ohm resistor in LVDS. PECL drivers require 220-ohm pull down resistors from each driver output, and a 100-ohm resistor across each receiver input.

Vendors such as *Texas Instruments and Fairchild specialize in both LVDS and PECL logic families. National Semiconductor also specializes in LVDS technology.*

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Summary of Logic Characteristics

PARAMETER	GTLP+	LVDS	PECL
Data Transfer Type	Single-Ended/Parallel	Differential/Serial	Differential/Serial
Data Rate	>400Mbps	>400Mbps	>400Mbps
Supply Current (typ.) outputs disabled at 100MHz. Data Rate	 40mA 200mA	 8mA 170mA	 40mA 300mA
Propagation Delay Driver Receiver	 3.8ns 3.8ns	 1.7ns 2.7ns	 4.5ns 7.0ns
Termination	Complex	Simple	Complex
EMI	GOOD	VERY GOOD	GOOD
Pulse Skew (typ.)	300ps	400ps	500ps
Hot Insertion	Yes	Yes	No
PCB/Connector Cost	Single Trace/Single Connector pin per signal	Pair of Traces/Pair of Connector pins + GND pin per signal	Pair of Traces/Pair of Connector pins

Figure 5: Comparison of Logic Families

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Backplane Connectors for High Speed Applications

As backplane data rates approach and exceed the gigabit per second threshold, it is critical to use backplane connectors that maintain signal integrity. How well these connectors are designed, will dictate how well the overall backplane system performs, in terms of line trace impedance, line discontinuities, signal distortion, cross-talk and noise.

Popular pin and socket connectors for single-ended transmission include VME type (DIN41612) and PCI type connectors (2mm "Hard Metric").

Some standard pin and socket connectors such as the *VHDM family* of connectors from Teradyne *(HSD-5 and HSD-8)* and the ERmetZD connector from Erni, were designed to handle high speed differential transmission at 2.5Gbps and beyond. They provide low cross talk, good trace routing capabilities, and short mating intervals, all for a 100-ohm differential-signaling environment. The connector housings usually have pre-alignment pins that help align the daughter-board and backplane connectors prior to contact engagement. There are options for 20, 25, 30, 38 and 40 differential paired signals.

For shelf-to-shelf connectivity in high-speed environments, AMP provides cable assemblies based on their CHAMP 0.8mm High Density Connector. The 0.8mm connector is fully shielded and contains two rows of molded contacts on 0.8mm centerlines. In LVDS applications, #30 AWG shielded-twisted pair wire is the recommended choice.

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Conclusions

Logic family choices:

1) PECL does not seem to have any advantage when compared with LVDS.
2) GTL or GTLP have the advantage of saving some backplane lines (many grounds are still needed).
3) LVDS: Requires doubling the signal pins for differential transmission. It has excellent noise immunity, good cross talk and very low EMI. Optimized for high-speed data transmission over longer distances (ex. long cables, longer backplanes).

Connector choices:

1) Hard Metric 2-mm: This is the type of connector used in cPCI applications. It has the advantage of being widely used and therefore has lower cost and multiple sources.
2) Teradyne-type (including Molex & AMP second sources): This family is specifically designed for differential transmission. It provides high signal density, very low cross talk and good EMI behavior. It also provides for integrated shielding in addition to signal pins.
3) ErmetZD: This type of connector is currently available from the joint venture partnership between Erni & Tyco Electronics (through its AMP division). This is an evolution of the Teradyne-type connector.

