ComSysDes

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Demystifying PCB Impedance Control

Practical PCB Formulas and Plots

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Scope of this Report

This report is the result of the need expressed by ComSysDes customers to have a handy reference for impedance control formulas and plots. The formulas presented here and its many variations have been in use in the PCB industry for years. The original paper was created using Mathsoft's MatchCAD tool. MathCAD's users can request a copy of the original paper by visiting http://ComSysDes.com . The interested reader can also create his/her own tools by entering the given formulas into a spreadsheet like Microsoft's Excel.

There are many sources in the World Wide Web that provide "electronic calculators" for some of the geometry cases. This documents provides the formulas and charts so the whole range of design alternatives can be quickly evaluated by the designer. In many cases, no additional calculations or resources will be needed.

This paper does not attempt to replace the help of the high speed signal integrity specialist. It is hoped, however, that it will help the digital designers in their dialog with the fab house with better understanding of the impedance control issues and the PCB fabrication process.

Brief Theoretical Introduction

This short paper addresses the needs of electrical and system designers that occasionally deal with impedance control problems in PCB design. Thus it attempts to provide a set of ready solutions for the most common geometry cases found in PCB design, mostly in the form of the impedance plots. The formulas are also shown so the interested reader can interpolate for values that the plots might not cover.

Characteristic impedance of a transmission line

Without getting deep into the theory we can say that a transmission line correctly terminated at one end behaves at the other end as if the terminating impedance was present there, with the only noticeable effect being a certain delay. This delay is the time that takes the electrical phenomena to travel over the transmission line and this speed is a fraction of the speed of light in vacuum, typically between 0.4 and 0.9.

This is to say that for a correctly terminated line will be no reflections distorting the waveform. The validity of these assertions is limited by some implicit assumptions, notably that the losses in the transmission line itself are negligible and that the characteristic impedance is essentially independent of the frequency in the spectrum of interest. These two approximations are justified in the typical situations and materials normally used in digital designs, so we can confidently use the results presented in here.

The general case of Capacitive Reactance and Inductive and Reactance is:

$$X_L(j\omega) := j\omega \cdot L \qquad X_C(j\omega) := \frac{-1}{j\omega \cdot C}$$

It can be shown that for a line without losses, the characteristic impedance is the positive square root of the product of the Inductive Reactance and the Capacitive Reactance per unit of length.

$$Z_0 := \sqrt{X_{L0} \cdot X_{C0}} \qquad Z_0 := \sqrt{\left(\frac{-1}{j\omega \cdot C_0}\right) \cdot (j\omega \cdot L_0)} \qquad Z_0 := \sqrt{\frac{L_0}{C_0}}$$

Since the two reactances are imaginary numbers of opposite sign it results that the characteristic impedance is a real number. In other words, it looks as a regular resistor but with the

peculiarity that it does not dissipate power. In fact the power is dissipated (with the delay as mentioned above) at the other end by the real resistor that terminates the line. Another consequence, shown in the third expression, is that even though the characteristic impedance is essentially a dynamic phenomenon, it can be calculated purely by static means. Those means depend of the inductance and capacitance per unit length, which in turn depend strictly of the geometry of the line in question.

The bad news is that there are no practical general expressions applicable to all line shapes. Only a handful of cases with simple geometry that admit exact analytical solutions. If an accurate impedance calculation is needed for an arbitrary geometry the best bet are the numerical methods. These methods work by successive numeric approximations applied to some deceptively simple equations satisfying the boundary conditions imposed by the geometry (metal and dielectric).

Fortunately, there are approximate or accurate enough solutions for a number of cases of interest. We will here concentrate of some of those cases, especially as it applies to common structures in PCB design. These are variations of the ubiquitous "microstrip" (trace over a dielectric over a ground plane) and "stripline" (trace buried in a dielectric, sandwiched between two ground planes).

The fact that the transmission line acts as if the load was directly present at the input (other than the delay phenomenon) is the reason why we are interested in its behavior in the realm of digital design. As result of its own nature, the waveform presented at its input makes its way to the output without reflections or distortions of any kind.

Some of the Jargon and Background

Core Construction: PCB fabrication process that piles up core materials with intermediate prepeg material. This method always results in an even number of layers.

Foil construction: PCB fabrication process similar to the Core Construction except in the external layers. The external layers are added using sheets of copper foil on top of prepeg material. Even though this method can theoretically produce odd number of layers it is recommended to still use an even number due to the risk of warpage and cost (it is usually cheaper to *add* a layer).

Prepeg: Short for pre-impregnated material. It consists of sheets of the basic material (for example, FR4) impregnated with a synthetic resin partially cured to an intermediate stage. Prepeg is used between sheets of core material for middle layers and with copper foil on top for external layers.

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Copper Clad or "Core Material":: It is one of the raw materials used by PCB fab houses. It consists of a layer of dielectric material (the most common is FR4) sandwiched between layers of copper on each face. The copper layers are generally of the same thickness. The copper thickness is usually expressed in terms of "oz.", or more correctly in "ounces per square foot". This unit is equivalent to 1.4-mil thickness (35 microns). Most digital circuit designs use substrates of a glass/epoxy composite known as FR-4. Commonly commercially available values of copper thickness are 0.5, 1, 2 & 3 oz.

FR4: Typical material used in digital design. FR4 is a glass fiber epoxy laminate. It is the most commonly used PCB material. "FR" stands for "Fire Retardant" (ANSI). It is usable up to frequencies in the order of 1 GHz, with losses increasing with the frequency. In digital designs, the losses are not that bad. In fact, the low Q (high loss) materials are preferred for these applications because thy help to dissipate the energy of reflections and other spurious distortions.

Padstack: The description of copper and dielectric layers constituting a PCB, specifying each thickness. It consists of a number of pre-peg, cores and copper layers. Since the optimum padstack is PCB fab technology dependent, it is always a good idea to check a proposed padstack with your PCB house.

Microstrip: Consists of a trace running on the surface of a PCB separated by one or more layers of dielectric material from a ground plane located underneath. It is also called "surface microstrip" to distinguish it from the "coated" or "embedded" variations.

Embedded Microstrip: Similar to the plain or "surface microstrip" but buried into the dielectric material.

Coated Microstrip: Similar to the "embedded microstrip", differing from it because of the dielectric thinness on top and the construction process. The dielectric on top is usually the solder mask coating the PCB surface. It is an extreme case of Embedded Microstrip with different dielectric constant than the material below. The impedance does not usually change significantly from the regular Microstrip case except in case of very thin traces, which change a few units percent.

Stripline: Trace running between two ground planes. See under the "symmetric" and "asymmetric" variations.

Symmetric Stripline: This geometry consists of a trace running between two ground planes located in layers above and below with the same dielectric thickness and material on both sides.

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Asymmetric Stripline: Similar to the symmetric stripline except that the dielectric thickness above and below the trace are different. The material is typically of the same kind.

Etching: Chemical process to remove the unwanted copper from a layer during the fab process. The copper face where the etching solution is applied results in extra etching compared with the copper layer facing the FR4 core. This effect may be important in case of very thick copper or very narrow traces.

Ground Plane: For the purpose of impedance control a well decoupled VCC plane is equivalent to a true ground plane.

Microstrip

Microstrip

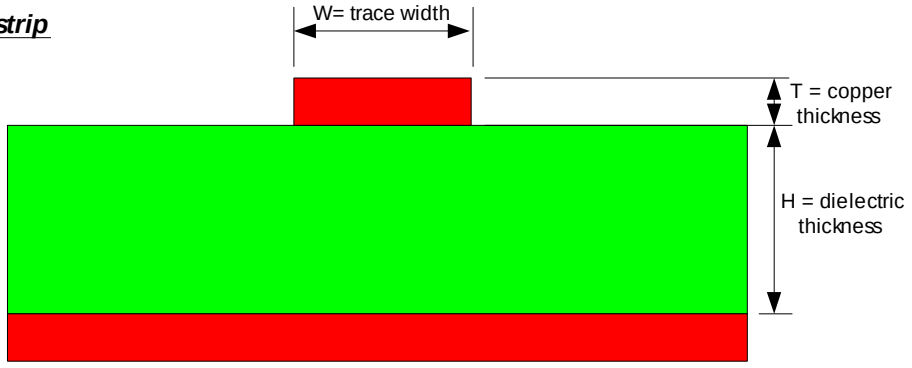

Figure 1: Microstrip Diagram

$$Z_0(W, H, T, \varepsilon_r) := \frac{87}{\sqrt{1.41 + \varepsilon_r}} \cdot \ln\left(\frac{5.98\,H}{T + 0.8\,W}\right)$$

$W := 4, 4.2 .. 12$ range for trace width

$\varepsilon_r := 4.2$ dielectric constant of the material

The following plot shows the impedance values for a couple of common values of the copper thickness (0.5 and 1 oz.) and typical FR4 material. The impedance is plotted against the trace width, for dielectric thickness from 4 through 14 mils and the plot is ordered by generally decreasing impedance.

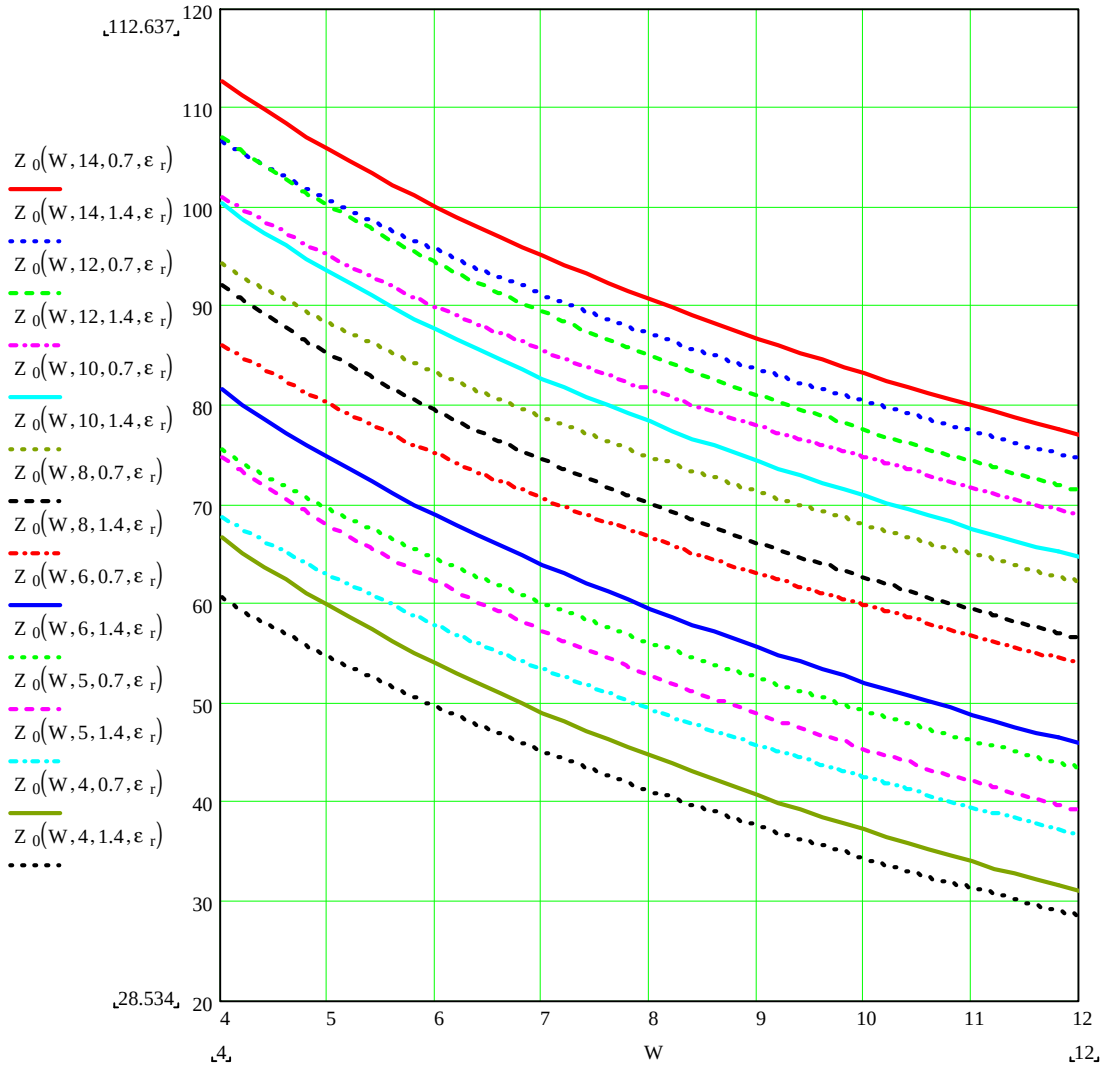

Figure 2: Microstrip Z_0, vs. trace width

Trace impedance shown as a function of trace width (W), dielectric thickness (H), trace thickness (H) and dielectric constant. The units are in mils.

Embedded Microstrip

Embedded Microstrip

Figure 3: Embedded Microstrip diagram

The formula to use in this case is the same as for the regular microstrip, adjusted to reflect the higher capacitance due to the presence of dielectric on top of the trace. This adjustment consists of defining a "virtual permitivity" that is a function of the ratio between the main dielectric thickness and the total dielectric thickness. The formula used in the industry is:

$$Z_0(W,H,H1,T,\varepsilon_r) := \frac{60}{\sqrt{\varepsilon_r \cdot \left(1 - \exp\left(-1.55 \cdot \frac{H1}{H}\right)\right)}} \cdot \ln\left(\frac{5.98 \cdot H}{T + 0.8 \cdot W}\right)$$

Here we see clearly that al these formulas should be taken as approximations and the specific geometry should be verified by coupon measurements. Notice that the equations for embedded microstrip T approaching zero and with H1 approaching H is not identical to the equation for the plain microstrip. Now, defining for convenience the "depth of embedding"

$$H2(H1,H,T) := H1 - T - H$$

$$Z_0(W,H,H2,T,\varepsilon_r) := \frac{60}{\sqrt{\varepsilon_r \cdot \left(1 - \exp\left(-1.55 \cdot \frac{H + H2 + T}{H}\right)\right)}} \cdot \ln\left(\frac{5.98 \cdot H}{T + 0.8 \cdot W}\right)$$

$W := 4, 4.2 .. 12$ range for trace width

$\varepsilon_r := 4.2$ dielectric constant of the material

The following plot shows the impedance values for a couple of common values of the copper thickness (0.5 and 1 oz.) and typical FR4 material, depth of embedding=14

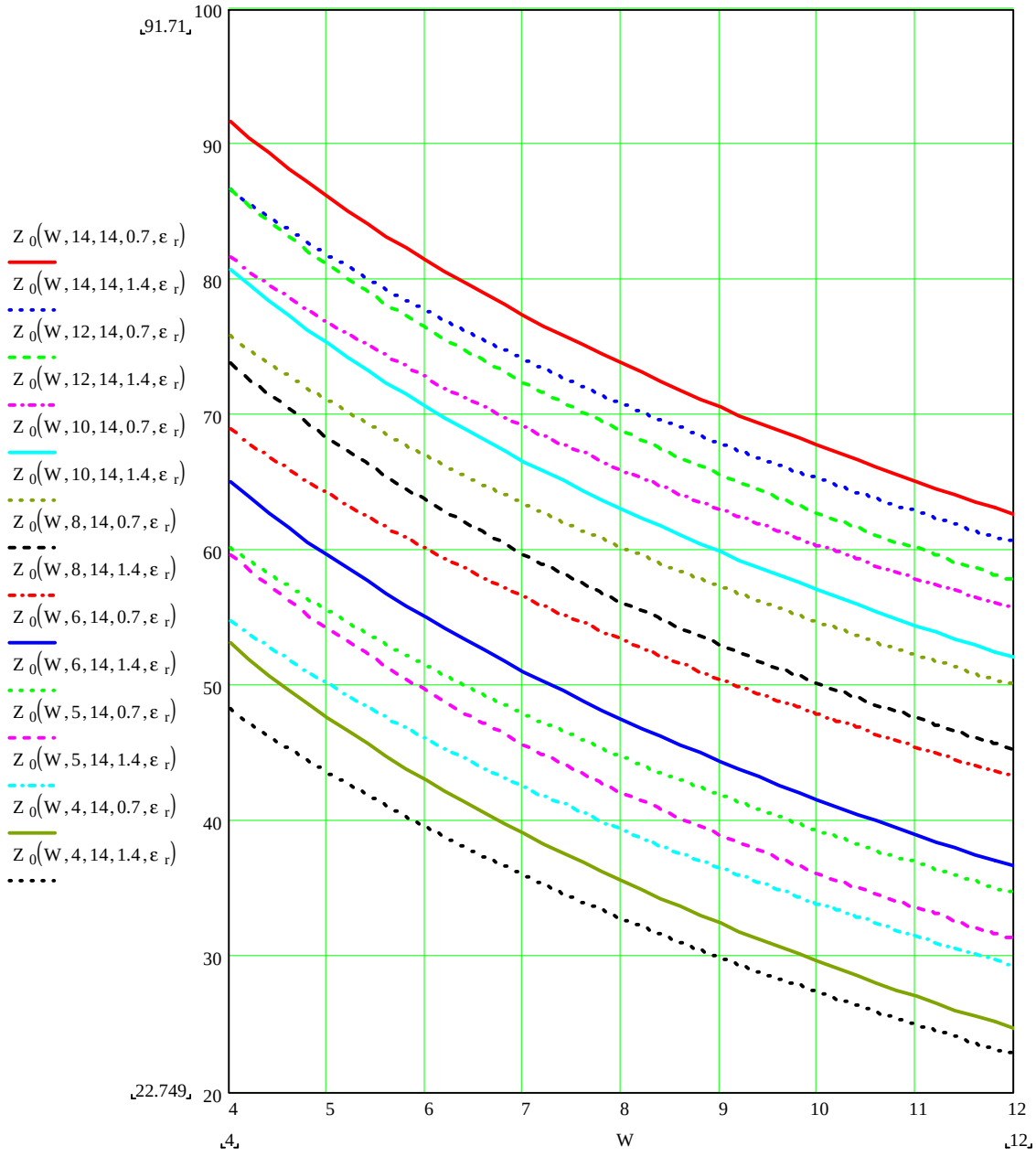

Figure 4: Embedded Microstrip Z_0 plot (embedding=14) vs. trace width

Trace impedance shown as a function of trace width (W), bottom dielectric thickness (H), top dielectric thickness (H2), trace thickness (H) and dielectric constant. The units are in mils.

The following plot shows is similar to the previous one but a deeper embedding, depth of embedding = 30. Notice the little change between both plots.

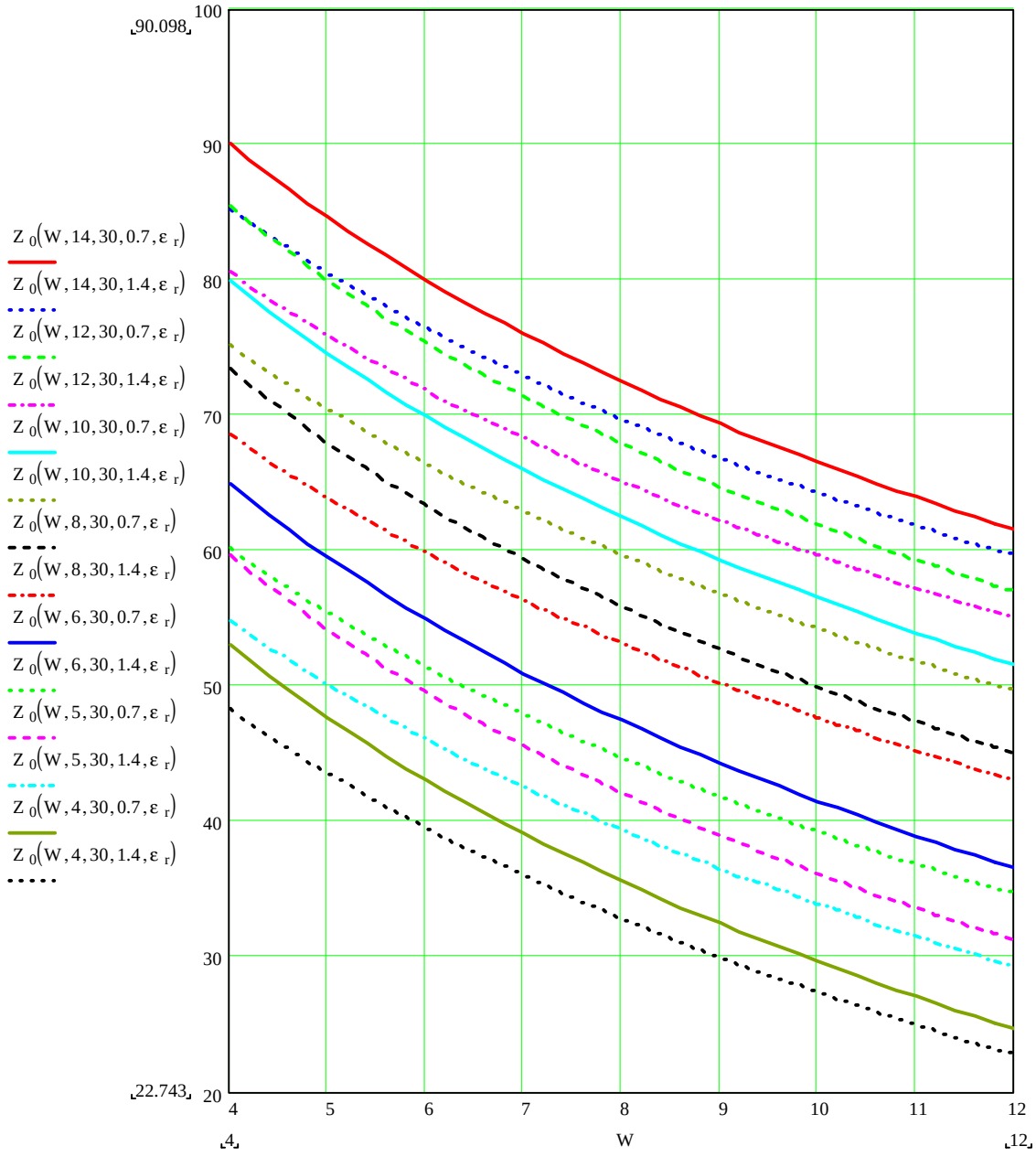

Figure 5: Embedded Microstrip Z_0 plot (embedding=30) vs. trace width

Trace impedance shown as a function of trace width (W), bottom dielectric thickness (H), top dielectric thickness (H2), trace thickness (H) and dielectric constant. The units are in mils.

Same as before, with shallower embedding (H2=10).

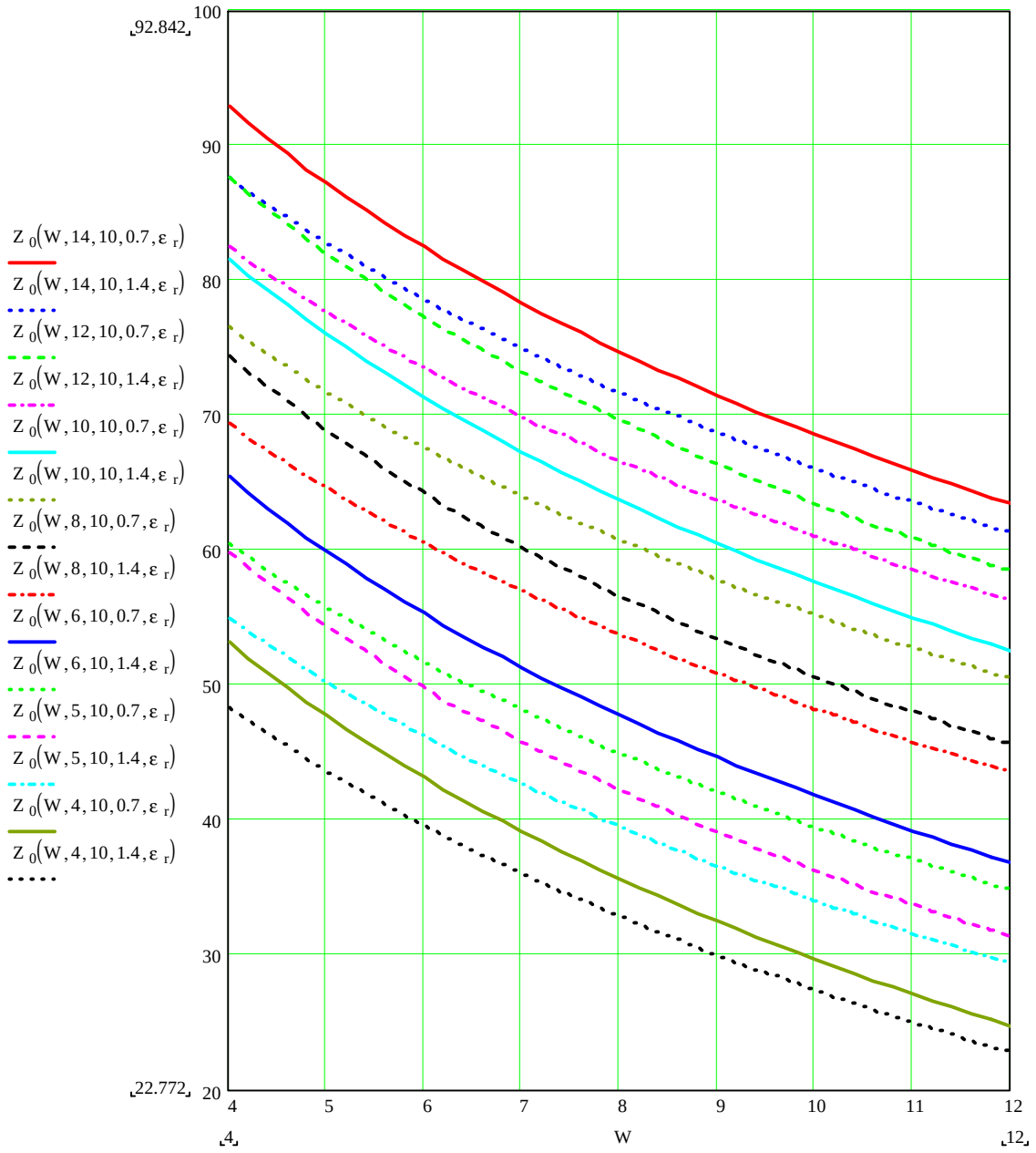

Figure 6: Embedded Microstrip Z_0 plot (embedding=10) vs. trace width

Trace impedance shown as a function of trace width (W), bottom dielectric thickness (H), top dielectric thickness (H2), trace thickness (H) and dielectric constant. The units are in mils.

Same as before, with shallower embedding (H2=8).

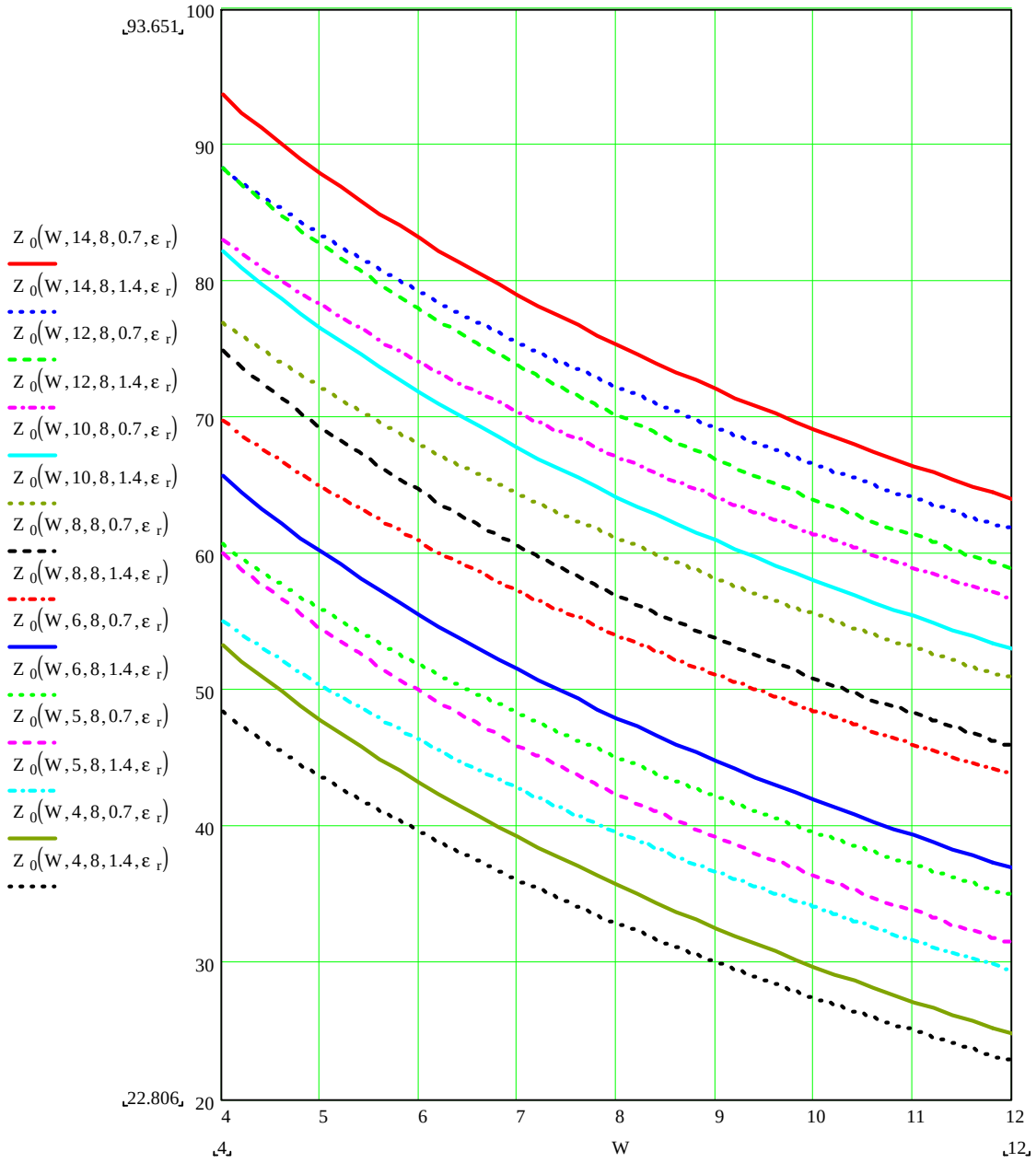

Figure 7: Embedded Microstrip Z_0 plot (embedding=8) vs. trace width

Trace impedance shown as a function of trace width (W), bottom dielectric thickness (H), top dielectric thickness (H2), trace thickness (H) and dielectric constant. The units are in mils.

Same as before, with shallower embedding (H2=6).

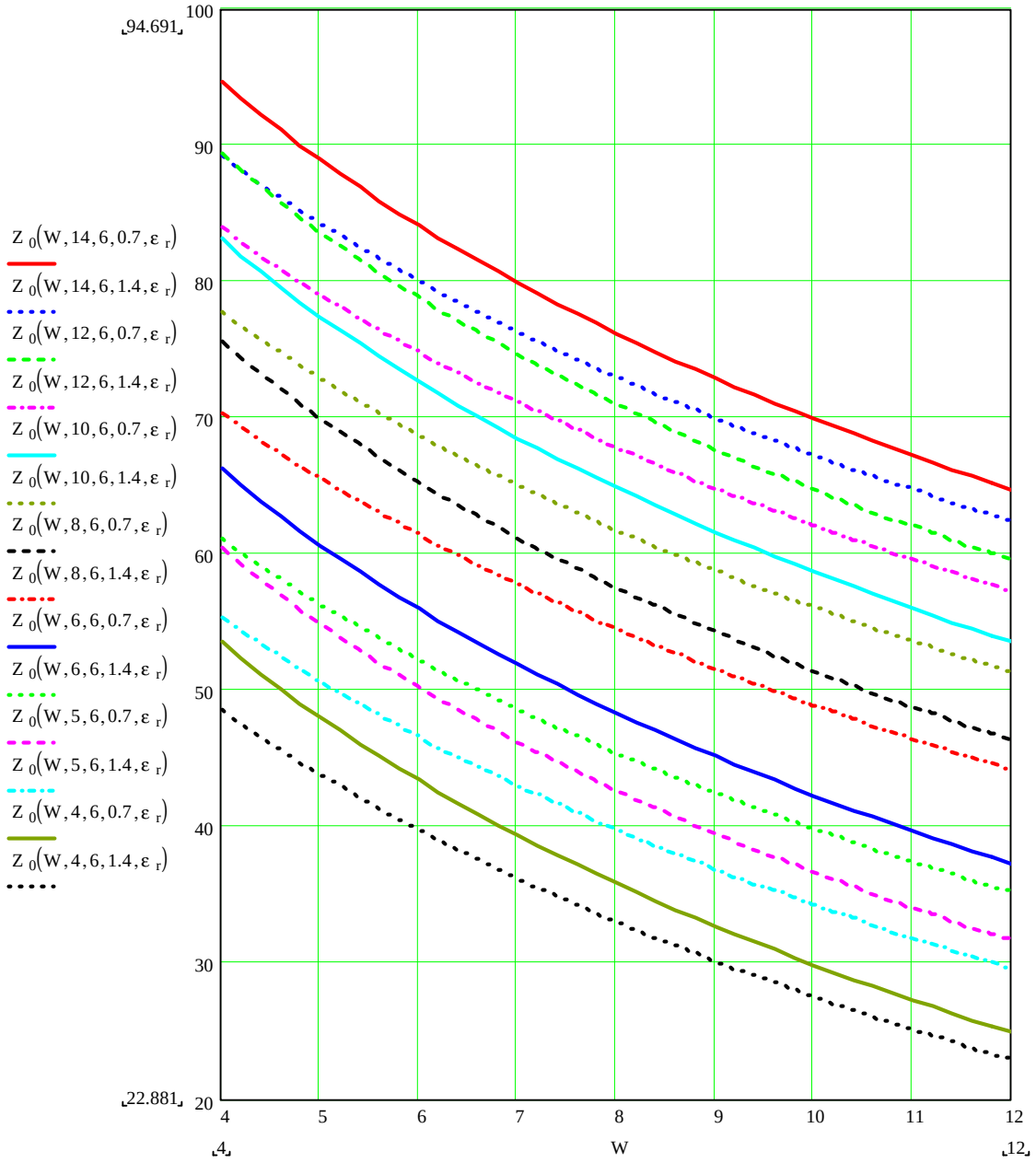

Figure 8: Embedded Microstrip Z_0 plot (embedding=6) vs. trace width

Trace impedance shown as a function of trace width (W), bottom dielectric thickness (H), top dielectric thickness (H2), trace thickness (H) and dielectric constant. The units are in mils.

Same as before, with shallower embedding (H2=4).

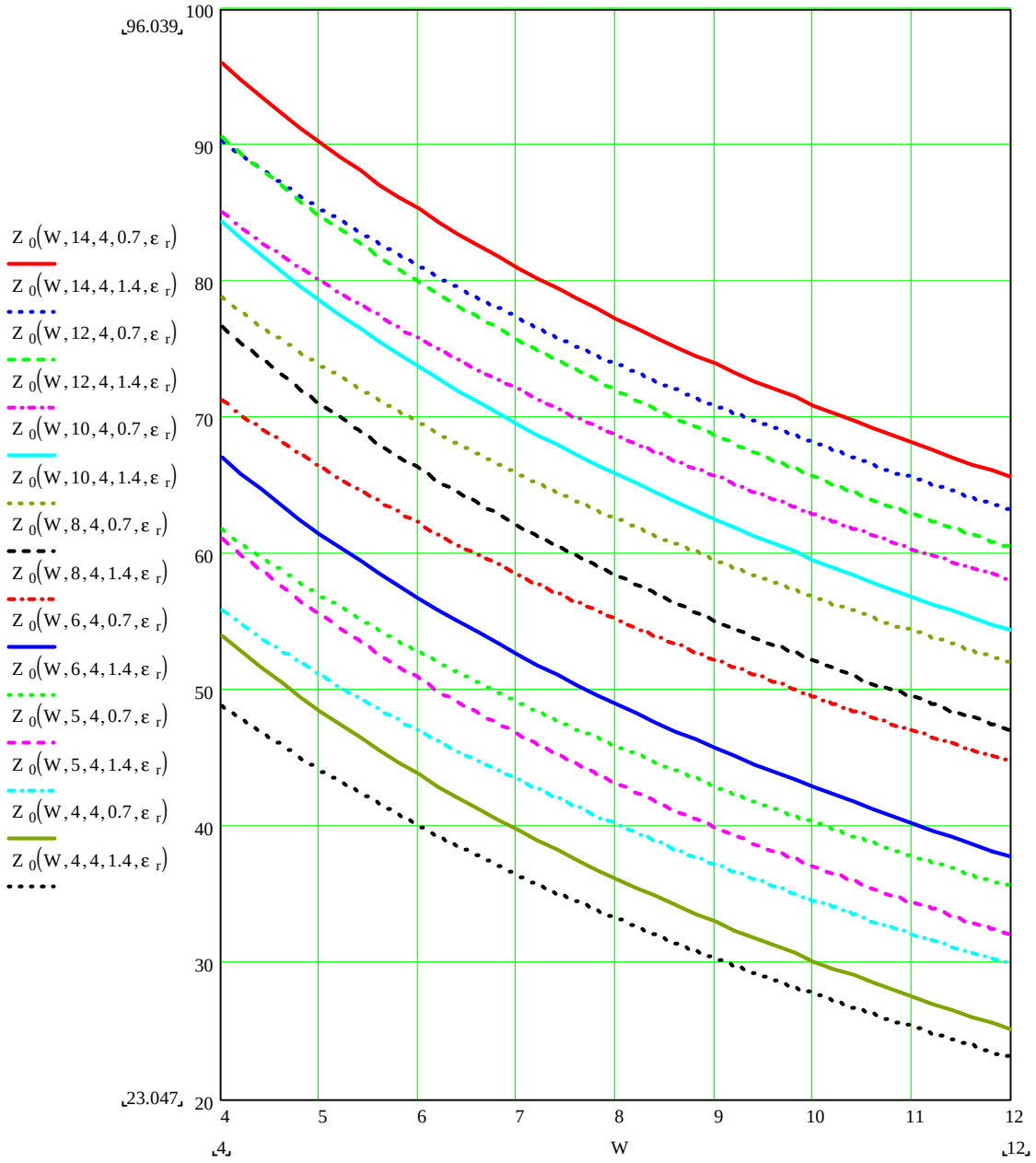

Figure 9: Embedded Microstrip Z_0 plot (embedding=4) vs. trace width

Trace impedance shown as a function of trace width (W), bottom dielectric thickness (H), top dielectric thickness (H2), trace thickness (H) and dielectric constant. The units are in mils.

Symmetric Stripline (Single Ended)

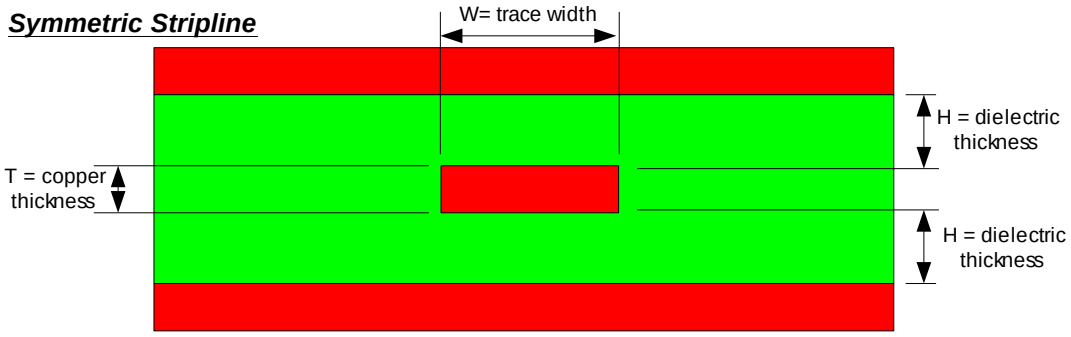

Figure 10: Symmetric Stripline diagram

$$Z_0(W, H, T, \varepsilon_r) := \frac{60}{\sqrt{\varepsilon_r}} \cdot \ln\left[1.9 \cdot \frac{(2 \cdot H + T)}{(0.8 \cdot W + T)}\right]$$

The following plots help in determining the single ended impedance of stripline geometry for the most common cases. For materials or dimensions not shown in these plots the impedance values can be calculated by using the above formula.

The plots are for the two most common copper thickness (1 oz. per s.f. is 1.4 mils thick, 1/2 oz. per s.f. is 0.7 mils thick) and the most common value of ε_r (dielectric constant) for FR4 material. The most common FR4 thickness values are 8 through 14 mils in increments of 2 mils.

Stripline impedance as function of trace width and dielectric thickness

$\varepsilon_r := 4.2$ dielectric constant of common FR4 material

$W := 4, 4.2.. 12$ common values for trace width

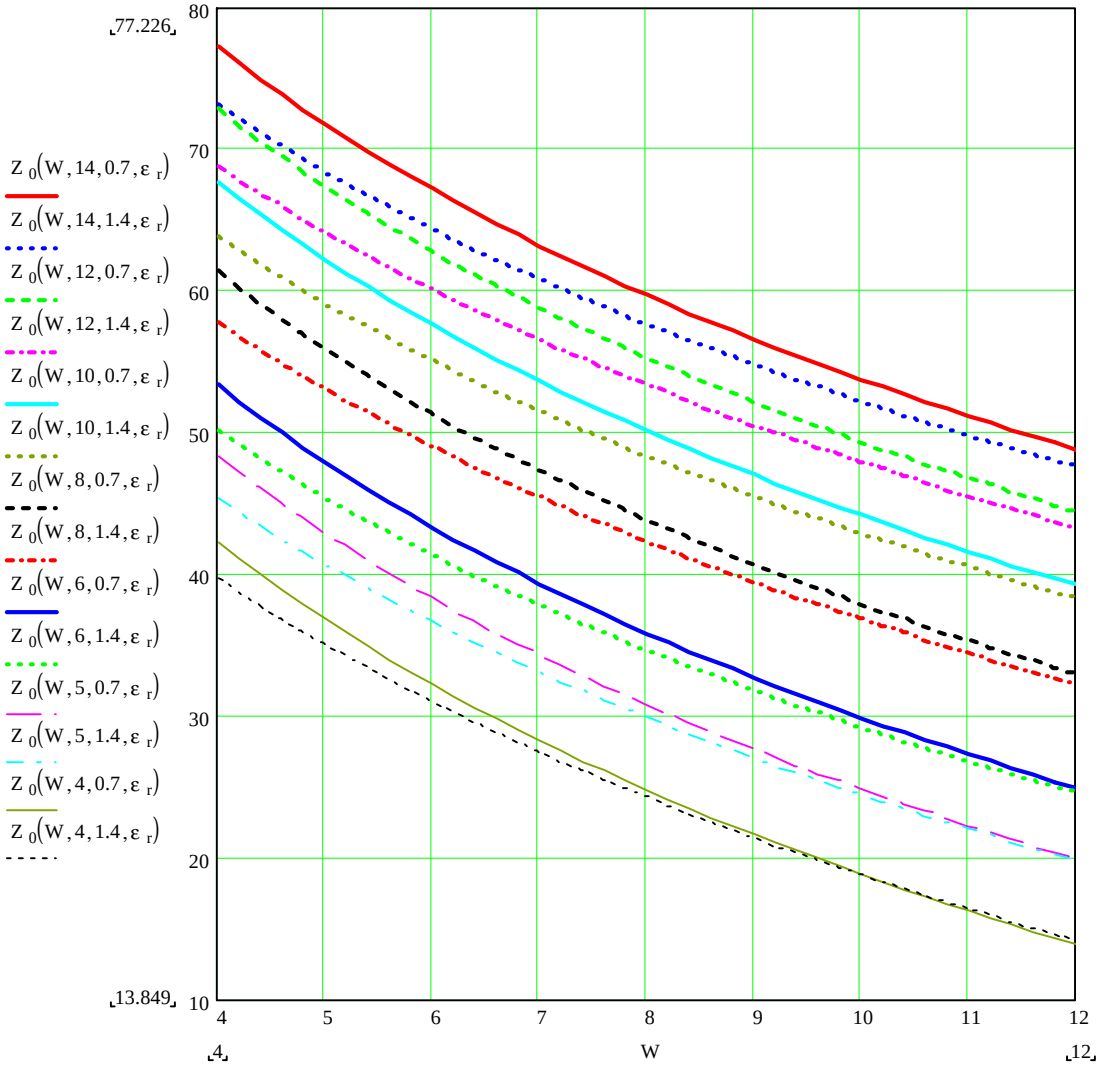

Figure 11: Symmetric stripline Z_0 plot, 4 through 14 mil trace width

The lowest curve is for the thinner FR4 and thicker copper (lower impedance for a given trace width), the highest curve is for thicker FR4 and thinner copper (highest impedance for a given trace width).

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Symmetric Stripline trace width as function of Z_0 and other Geometrical Dimensions

This is typically the problem that arises most frequently in practice. Given the parameters common for a whole layer (copper thickness, dielectric thickness, dielectric constant) we now set out to calculate the trace width necessary to obtain a given impedance:

$$W(Z_0, H, T, \varepsilon_r) := \frac{\frac{1.9 \cdot (2 \cdot H + T)}{\exp\left(\frac{Z_0 \cdot \sqrt{\varepsilon_r}}{60}\right)} - T}{0.8} \qquad Z_0 := 45, 46 .. 70 \qquad \varepsilon_r := 4.2$$

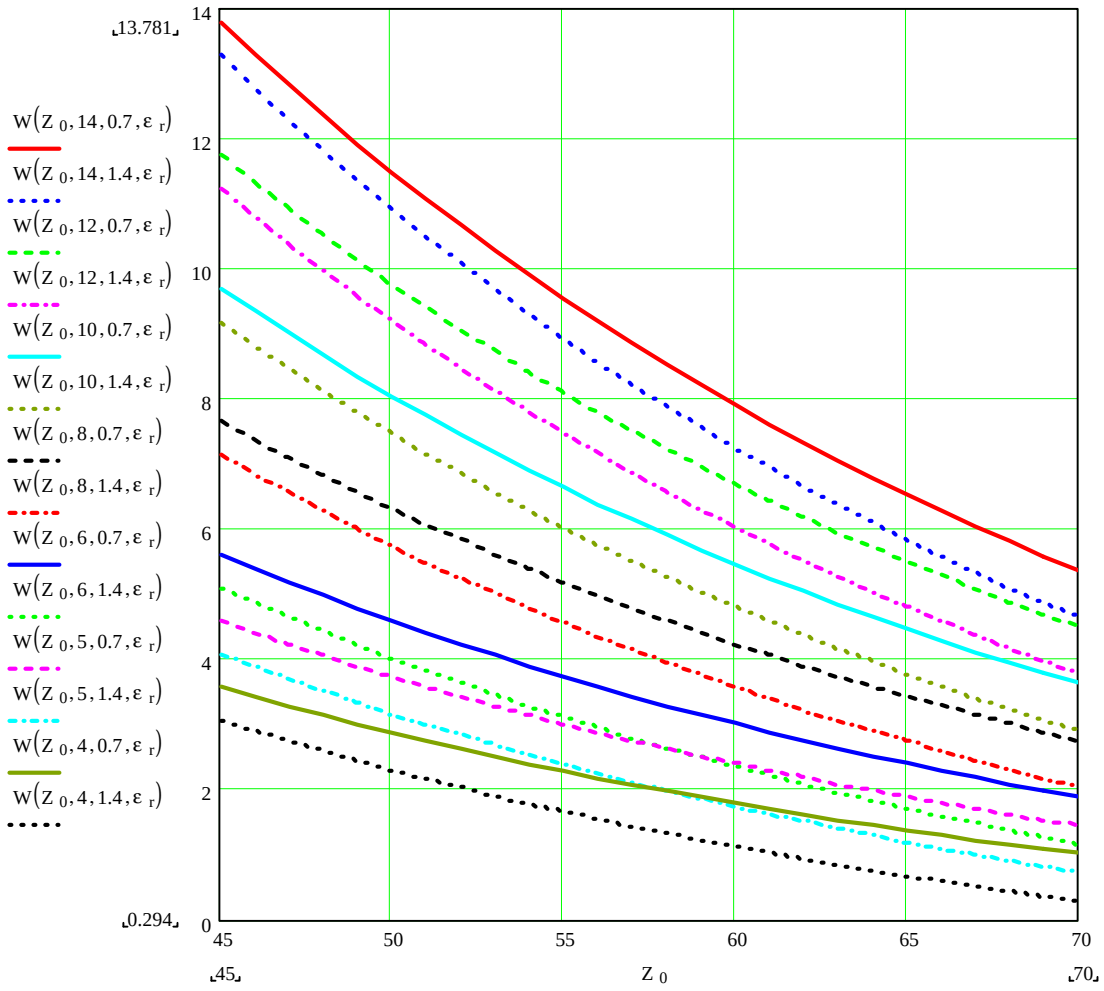

Figure 12: Symmetric stripline, trace width as function of desired Z_0

The lowest curve is for the thinner FR4 and thicker copper (narrower trace for a given impedance), the highest curve is for thicker FR4 and thinner copper (wider trace for a given impedance). Notice that trace widths smaller than 4 or 5 mils are currently hard to achieve in commercial PCB's with the normally used processes in the industry as of this date (August 2001).

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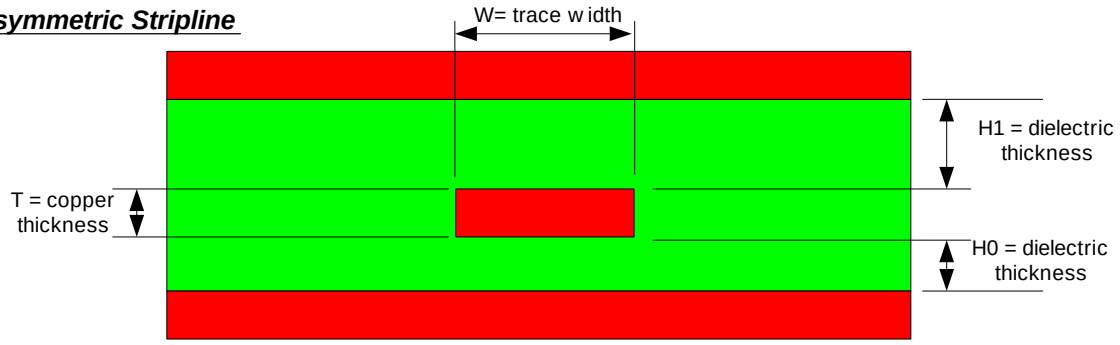
Asymmetric Stripline (Single Ended)

Asymmetric Stripline



$$Z_0(W, H_1, H_0, T, \varepsilon_r) := \frac{80}{\sqrt{\varepsilon_r}} \cdot \ln\left[1.9 \cdot \frac{(2 \cdot H_0 + T)}{(0.8 \cdot W + T)}\right] \cdot \left(1 - \frac{H_0}{4 \cdot H_1}\right)$$

$\varepsilon_r := 4.2$ dielectric constant of common FR4 material

$W := 4, 4.5 .. 12$ common values for trace width

NOTE: in the above formula H1 is always the larger value and H0 is the smaller.

The following plot shows all the combinations of dielectric thickness from 6 to 14 mils in increments of 2 mils for 1/2 oz copper. The combinations are in order of decreasing impedance

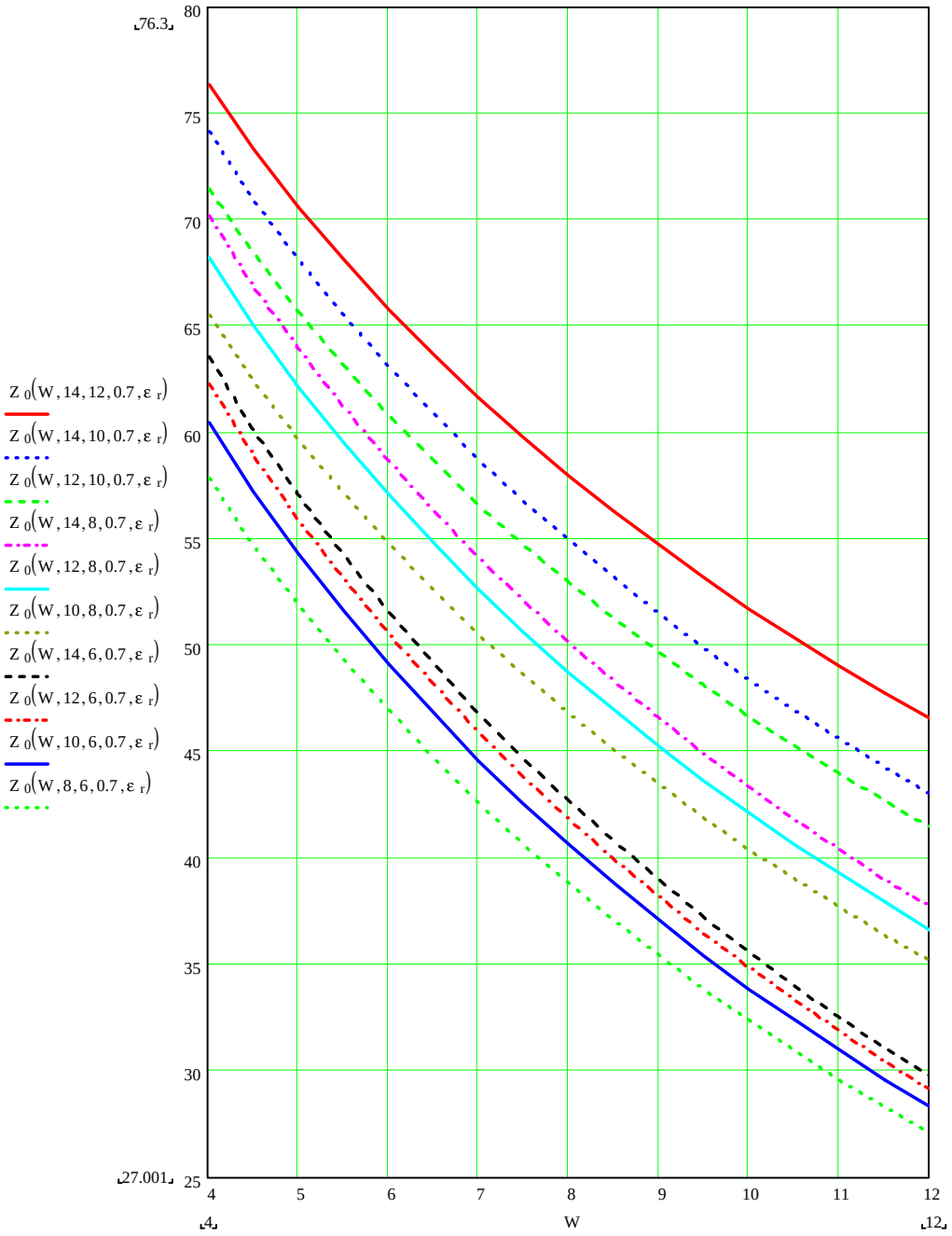


Figure 13: Asym stripline, 0.5 oz. copper, 6 to 14 mil dielectric combinations

The following plot shows all the combinations of 0.5 oz copper and 5 mil dielectric thickness in the thin side and 6, 8, 10, 12 and 14 mils dielectric thickness in the thick side.

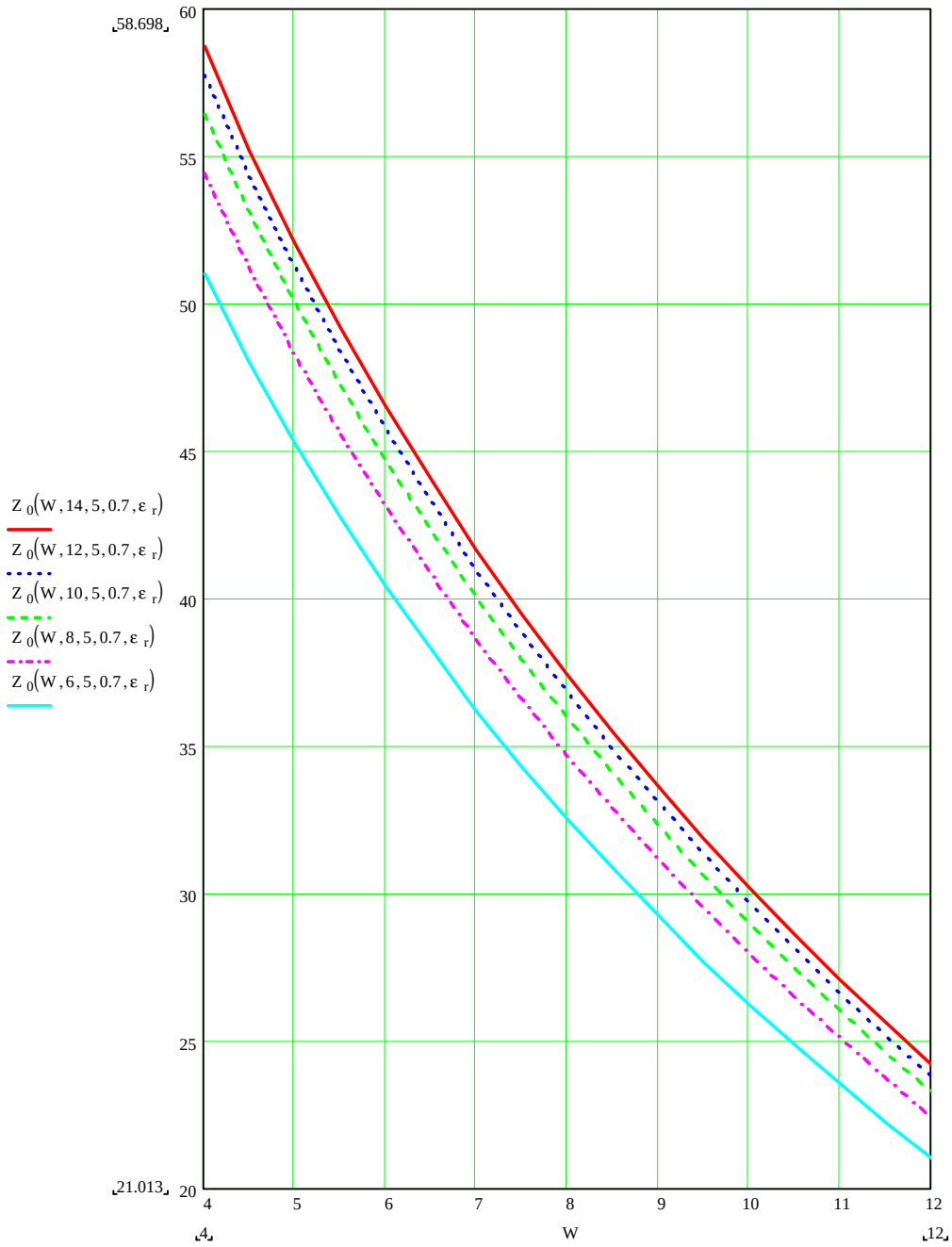


Figure 14: Asym stripline, 0.5 oz. copper, dielectric 5 mil with 6 through 14 mil

The following plot shows all the combinations of 0.5 oz copper and 4 mil dielectric thickness in the thin side and and 5, 6, 8, 10, 12 and 14 mils dielectric thickness in the thick side.

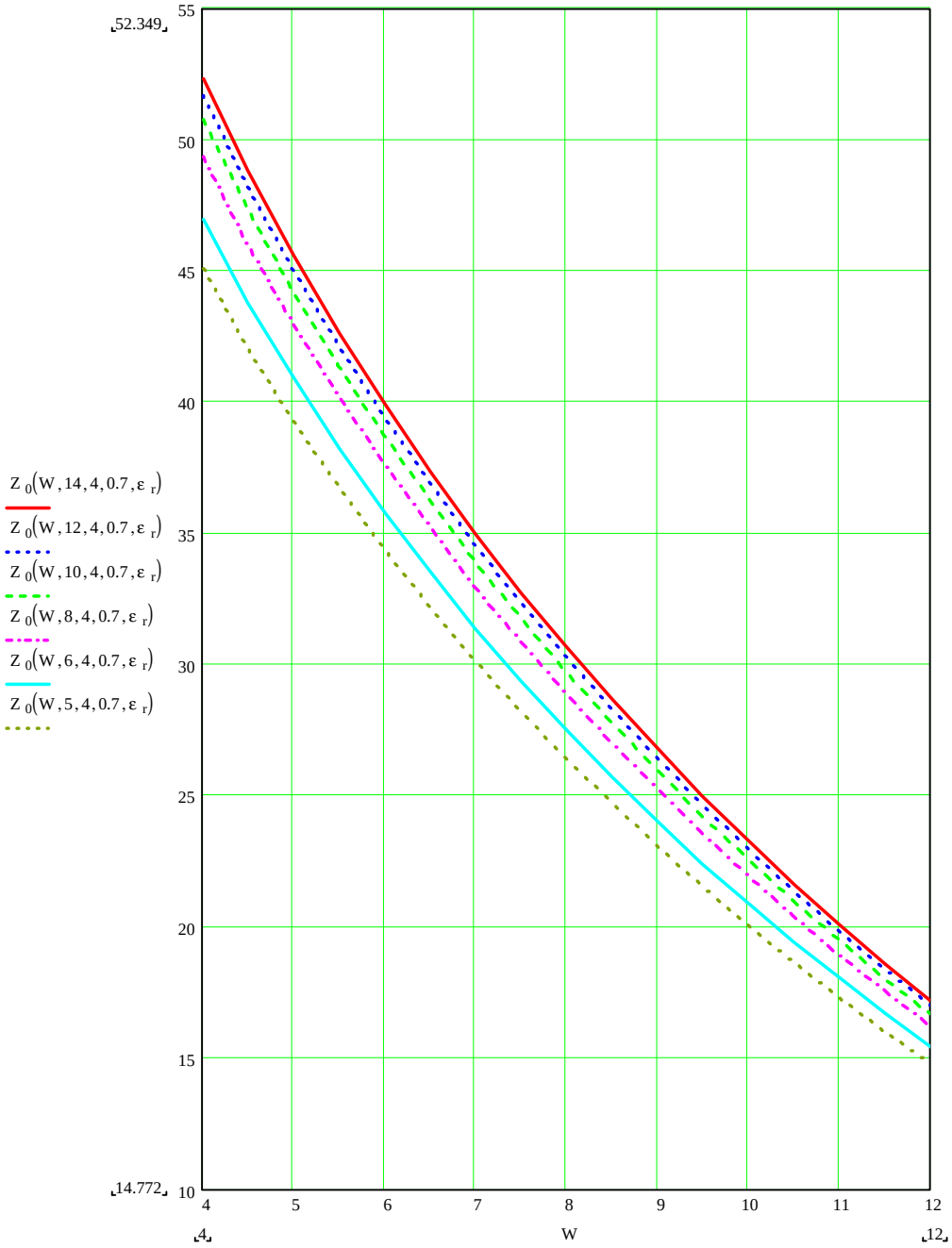


Figure 15: Asym stripline, 0.5 oz. copper, dielectric 4-mil with 5 through 14-mil

The following plot shows all the combinations of dielectric thickness from 6 to 14 mils in increments of 2 mils for 1 oz copper. The combinations are in order of decreasing impedance

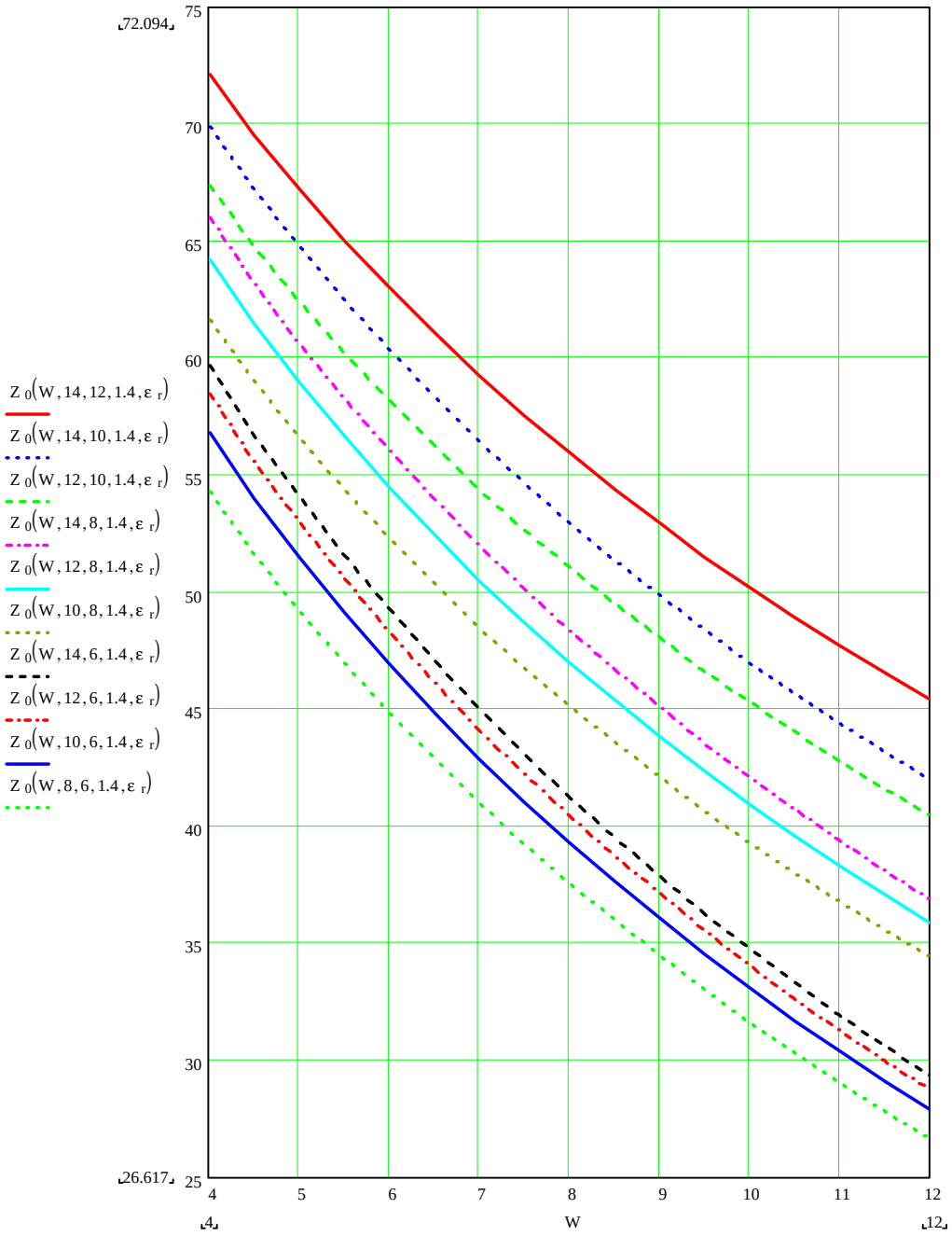


Figure 16: Asym stripline, 1 oz. copper, 6 to 14 mil dielectric combinations

The following plot shows all the combinations of 1 oz copper and 5 mil dielectric thickness in the thin side and 6, 8, 10, 12 and 14 mils dielectric thickness in the thick side.

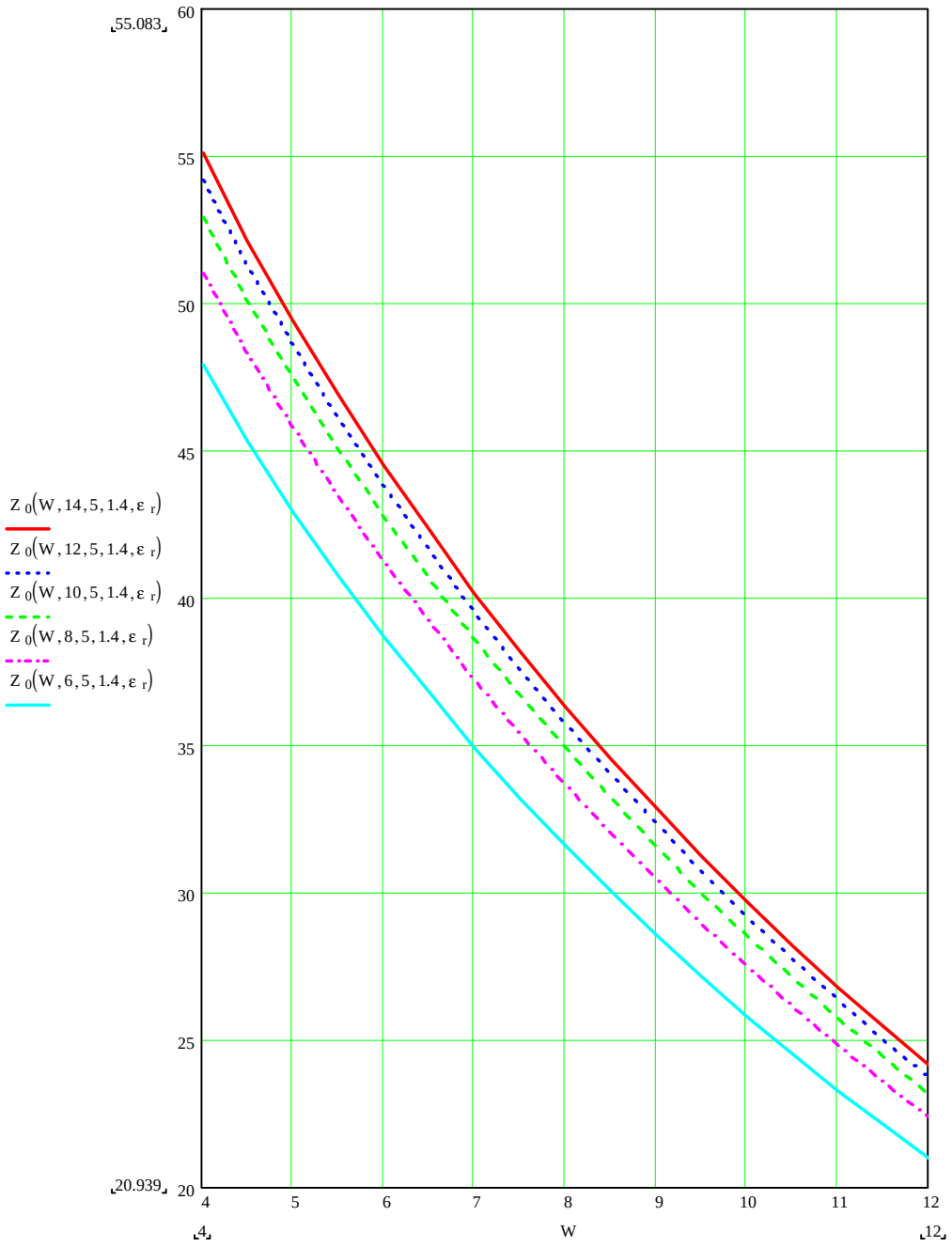


Figure 17: Asym stripline, 1 oz. copper, 5-mil with 6 through 14-mil dielectric

The following plot shows all the combinations of 1 oz copper and 4 mil dielectric thickness in the thin side and 5, 6, 8, 10, 12 and 14 mils dielectric thickness in the thick side.

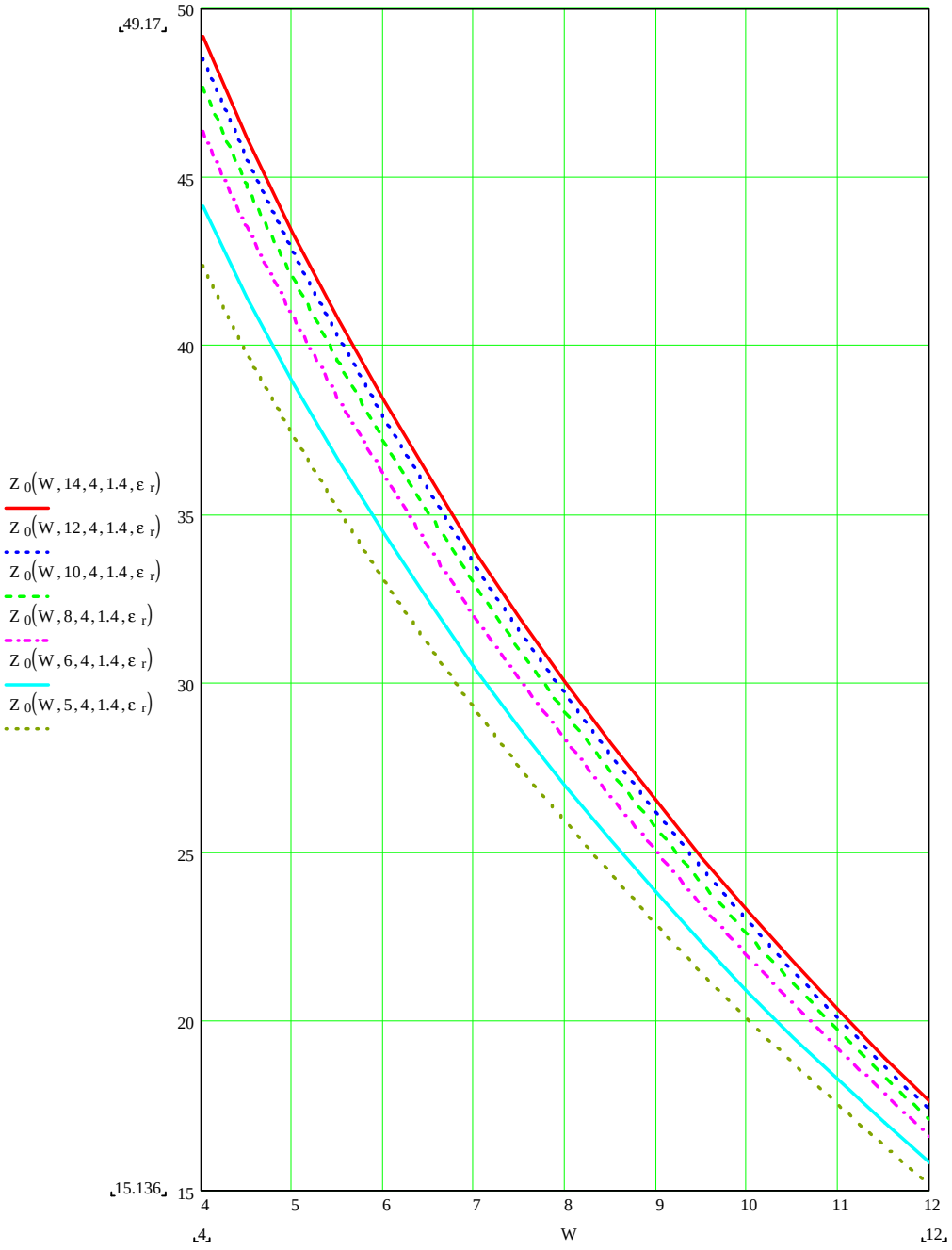


Figure 18: Asym stripline, 1 oz. copper, dielectric 4-mil with 5 through 14-mil

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Closing Notes

1) For dielectric constants different than 4.2 (the one assumed in this document) the impedance can be calculated by considering

$$Zo(e) = Zo(plot) \times \sqrt{4.2/e}$$

2) It has been remarked along this document that most the formulas presented here are only approximations to the real impedance values. Differences in the order of 5 or 10% could happen, especially in the asymmetrical microstrip case when the dielectric thickness at both sides is very different and in some cases of the embedded microstrip.

3) The formulas and plots in this document are valid only for the "single ended" mode. The impedance in differential mode is generally ***not*** equivalent to twice the single ended impedance unless the traces are very far apart (missing most of the benefits of differential transmission). Since there are additional independent variables compared with the single ended case it results in significantly increased number of charts and formulas. In many cases, the errors introduced in the approximate formulas require the use of numeric methods instead. Should you be interested in these cases please e-mail to Mktg@ComSysDes.com describing your specific geometry. The calculation will be sent at no charge if available on file. Otherwise, a quote for calculating the specific case will be sent instead.

4) The formulas and charts do not take into account the etching effect, which results in different trace width at the top and bottom of the traces. This effect becomes significant in the impedance calculations for thick copper, narrow traces or thin dielectric. Numerical methods are again the preferred way of solving these cases. Since the actual trace dimensions are very much dependent on the PCB fabrication process in these cases it is specially important to verify the actual impedance in the PCB themselves (for example, by using test coupons).

5) User feedback to improve the usefulness of this document is encouraged and appreciated.

